US005825677A

# United States Patent [19]

Agarwal et al.

[11] Patent Number: 5,825,677

[45] Date of Patent: Oct. 20, 1998

[54] **NUMERICALLY INTENSIVE COMPUTER ACCELERATOR**

[75] Inventors: **Ramesh Chandra Agarwal**, Yorktown Heights, N.Y.; **Randall Dean Groves**, Austin, Tex.; **Fred Gehrung Gustavson**, Briarcliff Manor, N.Y.; **Mark Alan Johnson**, Austin; **Brett Olsson**, Round Rock, both of Tex.

[73] Assignee: **International Business Machines Corporation**, Armonk, N.Y.

[21] Appl. No.: **619,456**

[22] Filed: **Mar. 20, 1996**

**Related U.S. Application Data**

[63] Continuation of Ser. No. 217,533, Mar. 24, 1994, abandoned.

[51] **Int. Cl.**[6] ..... **G06F 17/16**

[52] **U.S. Cl.** ..... **364/736.03**

[58] **Field of Search** ..... 364/736, 736.03

[56] **References Cited**

U.S. PATENT DOCUMENTS

| | | | |
|---|---|---|---|
| 4,594,682 | 6/1986 | Drimak | 364/736 |
| 4,617,625 | 10/1986 | Nagashima et al. | 364/200 |
| 4,621,324 | 11/1986 | Ushiro et al. | 364/200 |
| 4,685,076 | 8/1987 | Yoshida | 364/736 |
| 4,712,175 | 12/1987 | Torii et al. | 364/736 |
| 4,725,973 | 2/1988 | Matsuura et al. | 364/736 |
| 4,761,754 | 8/1988 | Kinoshita | 364/736 |
| 5,010,477 | 4/1991 | Omoda et al. | 364/200 |
| 5,274,818 | 12/1993 | Vasilevsky et al. | 395/700 |

FOREIGN PATENT DOCUMENTS

| | | |
|---|---|---|
| 0085435 | 8/1983 | European Pat. Off. . |
| 0195245 | 9/1986 | European Pat. Off. . |
| 0517013 | 12/1992 | European Pat. Off. . |

OTHER PUBLICATIONS

NEC Research and Development, No. 96, Mar. 1990, pp. 93–109, XP 000136298, "Mainframes and Their Related Products".

*Primary Examiner*—David H. Malzahn

*Attorney, Agent, or Firm*—Daniel P. Morris

[57] **ABSTRACT**

A matrix processing unit is described which permits high speed numerical computation. The processing unit is a vector processing unit which is formed from a plurality of processing elements. The Ith processing unit has a set of N registers within which the Ith elements or words of N vectors of data are stored. Each processing element has an arithmetic unit which is capable of performing arithmetic operations on the N elements in the set of N registers. Each vector of data has K elements. Therefore, there are K processing elements. A vector operation of the matrix processing unit simultaneously performs the same operation on all elements of two vectors or more. A subsequent vector operation can be performed within one machine cycle time after the preceding vector operation.

**16 Claims, 5 Drawing Sheets**